

FIG. 3

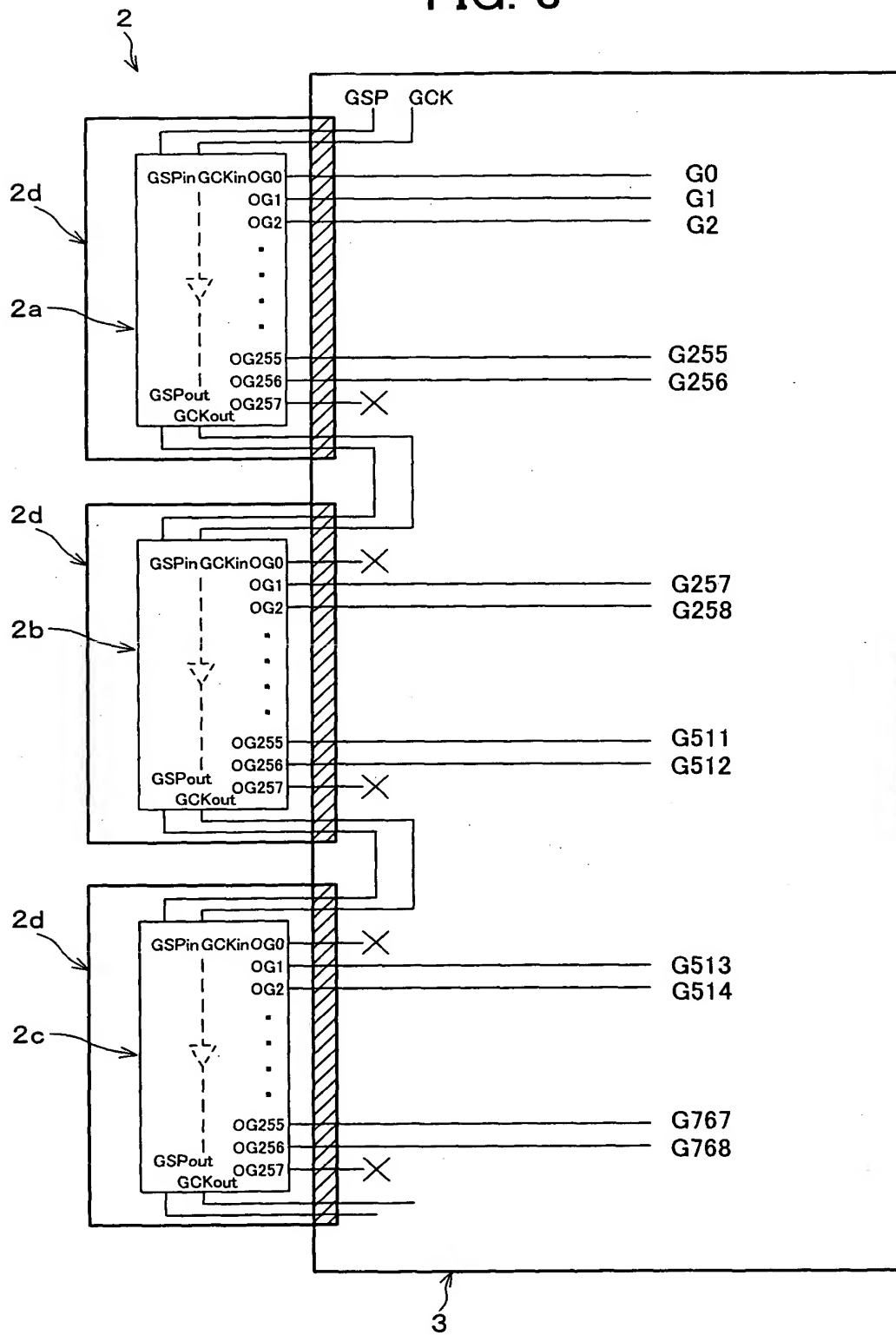


FIG. 4

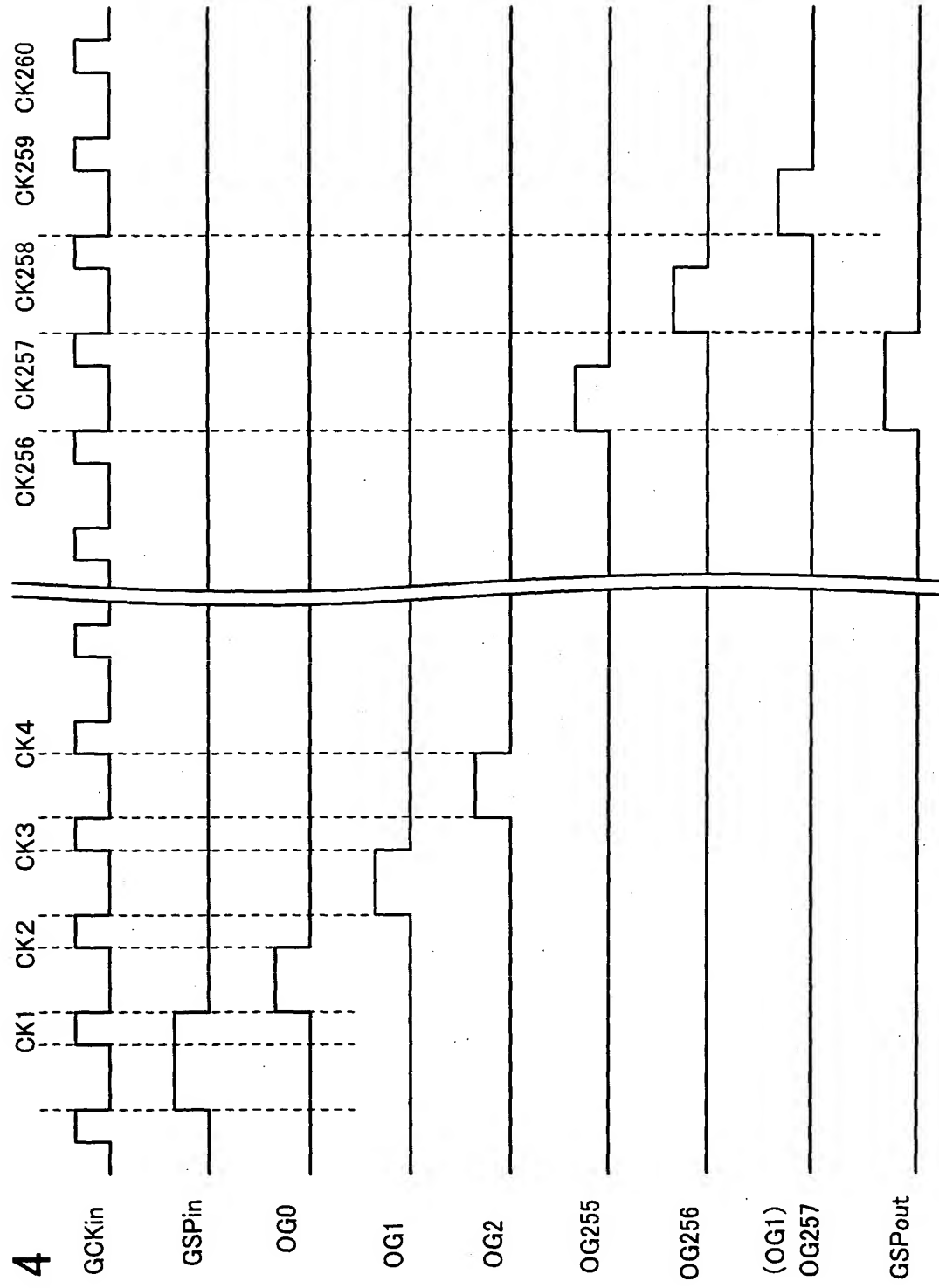


FIG. 5

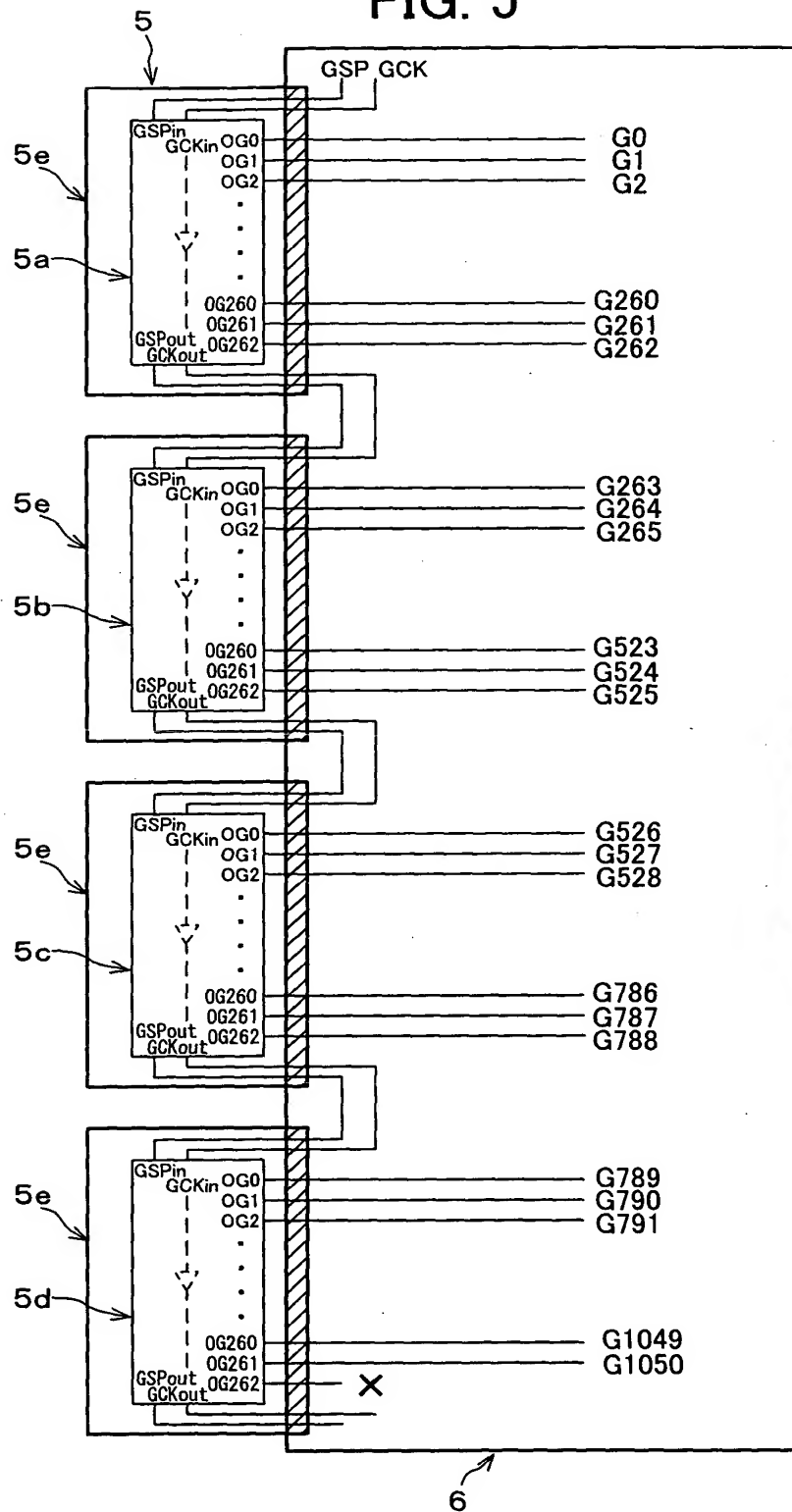
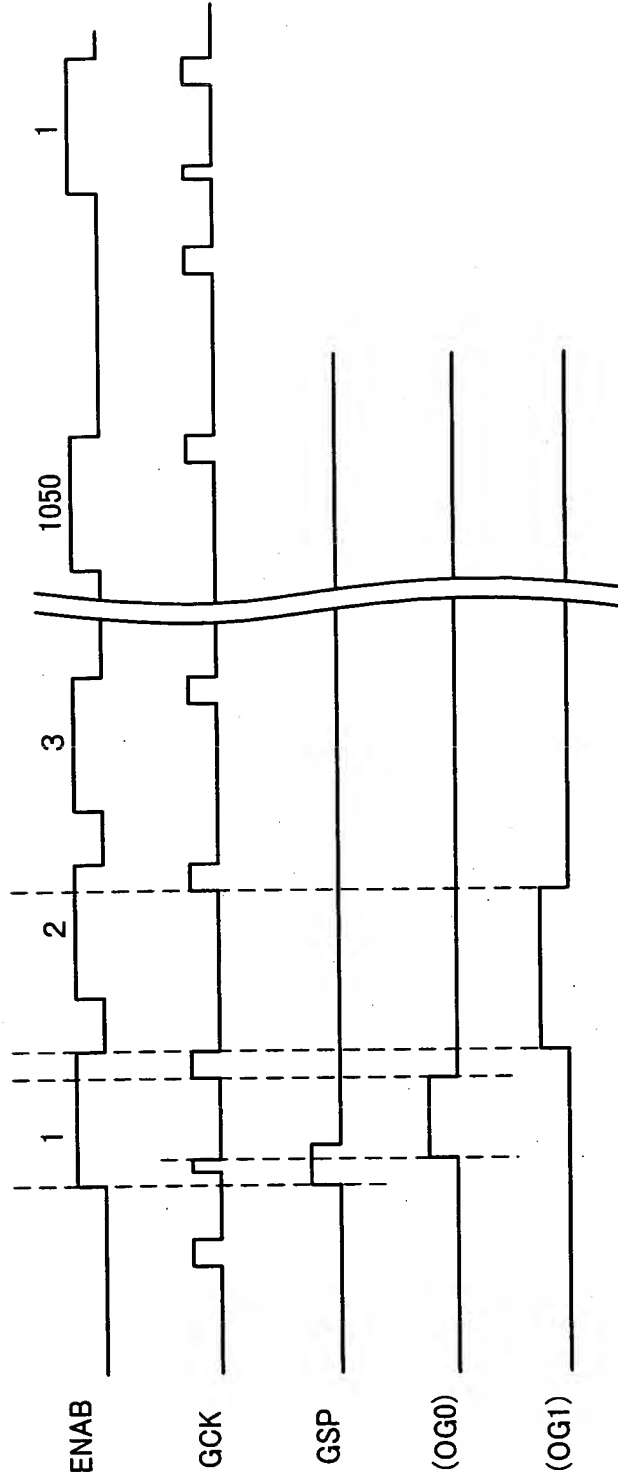


FIG. 6



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Timing diagram showing signals GCKin, GSPin, OG0, OG1, OG2, OG260, OG261, OG262, and GSPout. The diagram includes a clock signal CK with phases CK1 through CK265. A vertical line separates the input signals (left) from the output signals (right).

FIG. 8

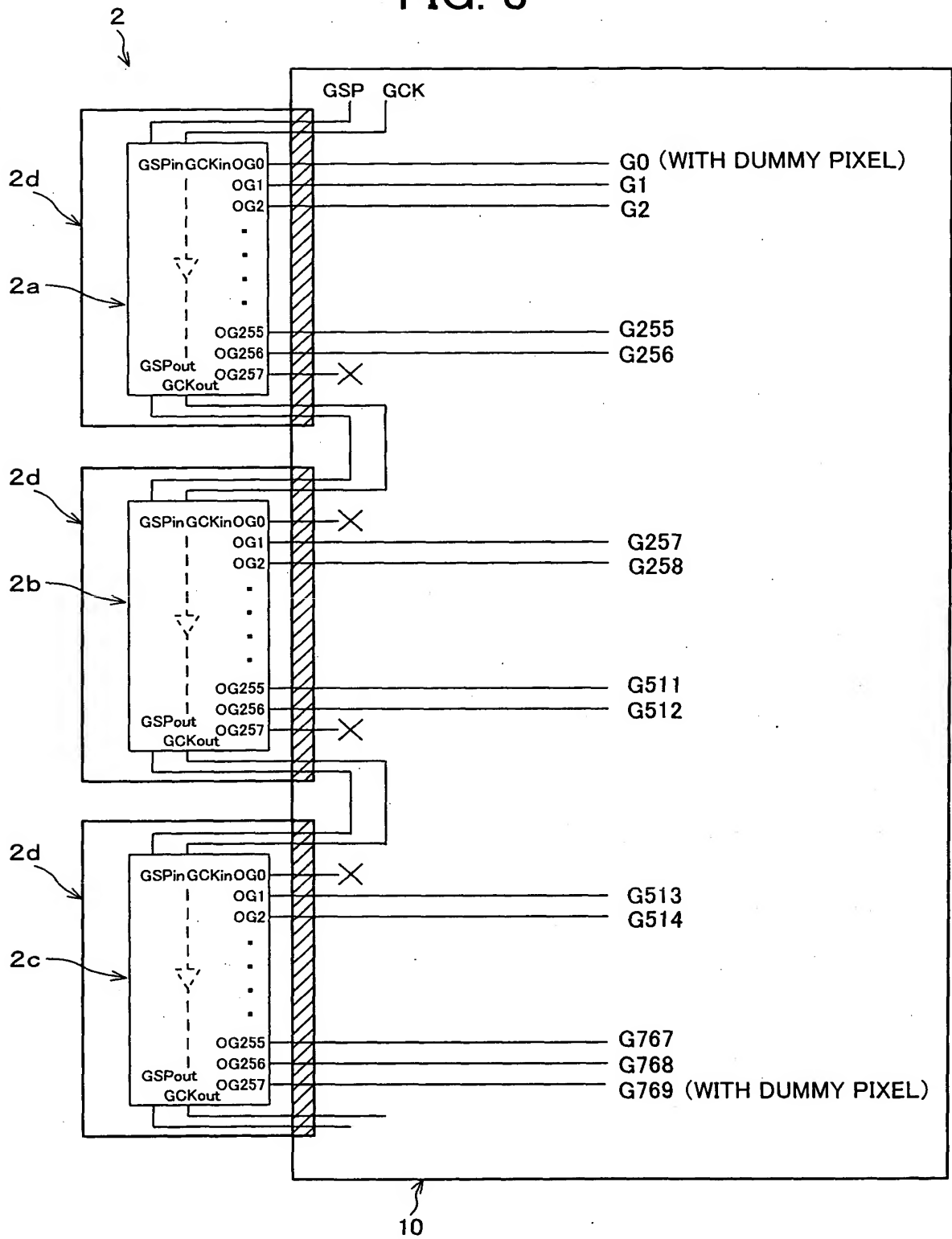


FIG. 9

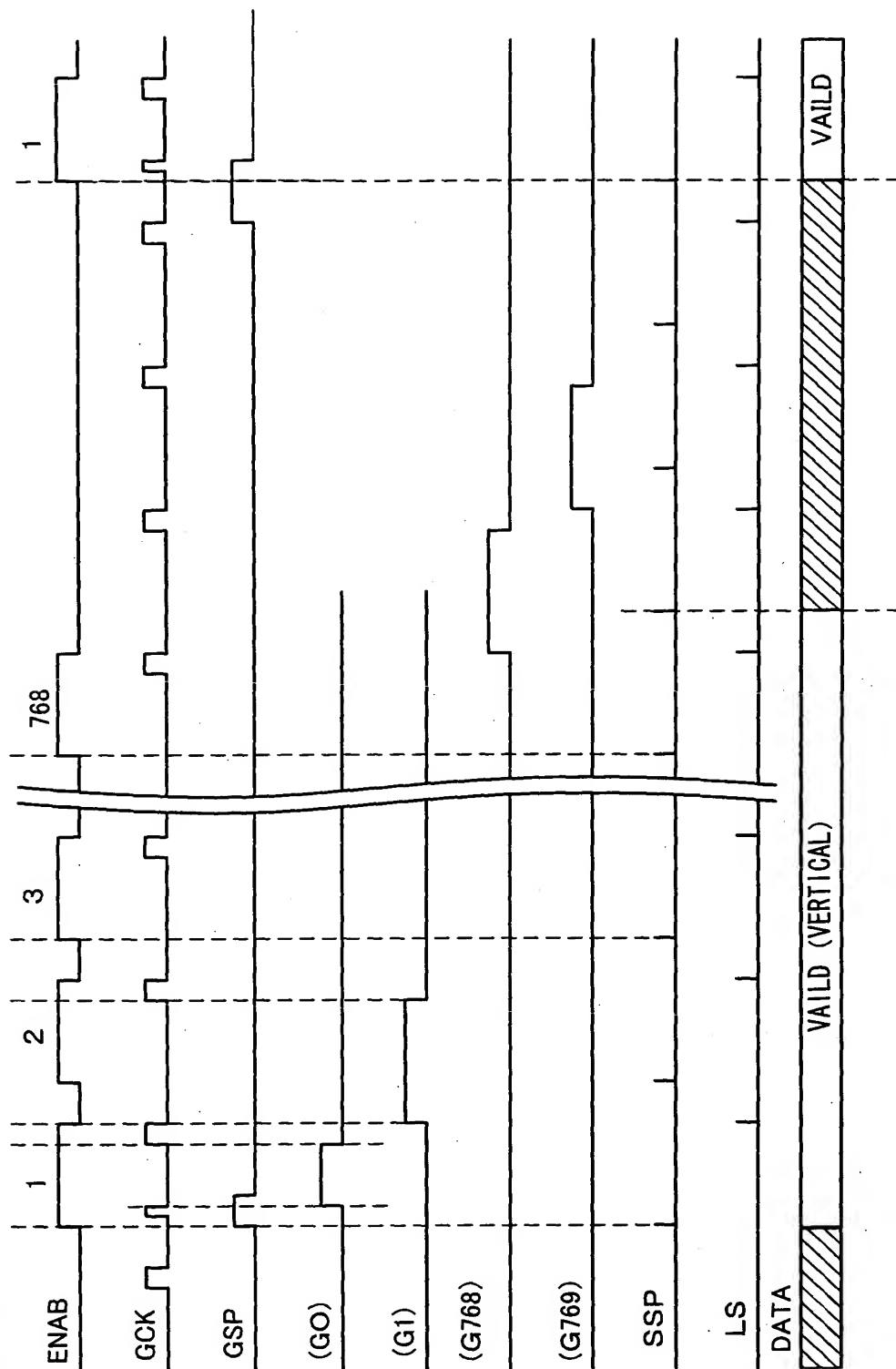


FIG. 10

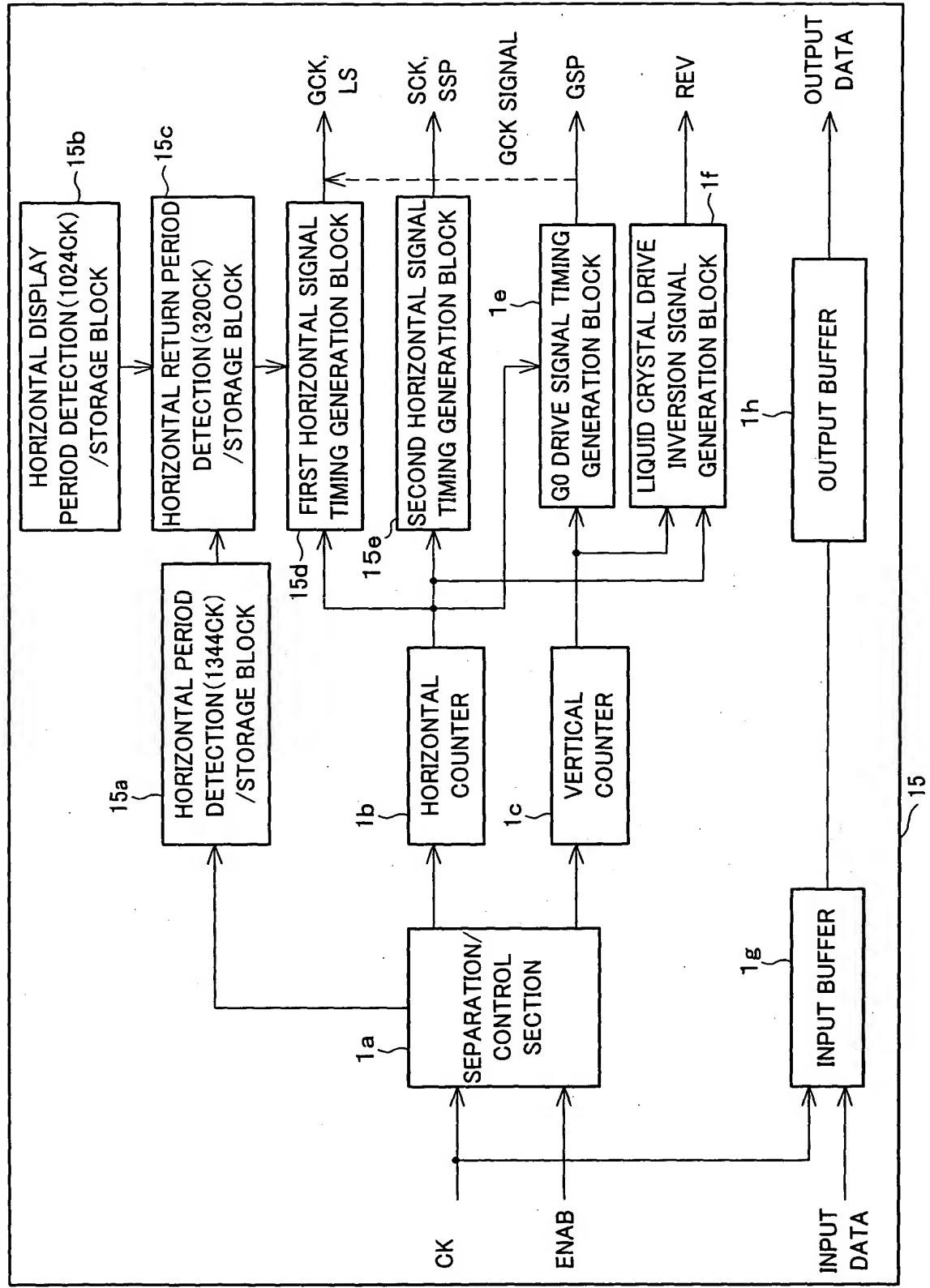
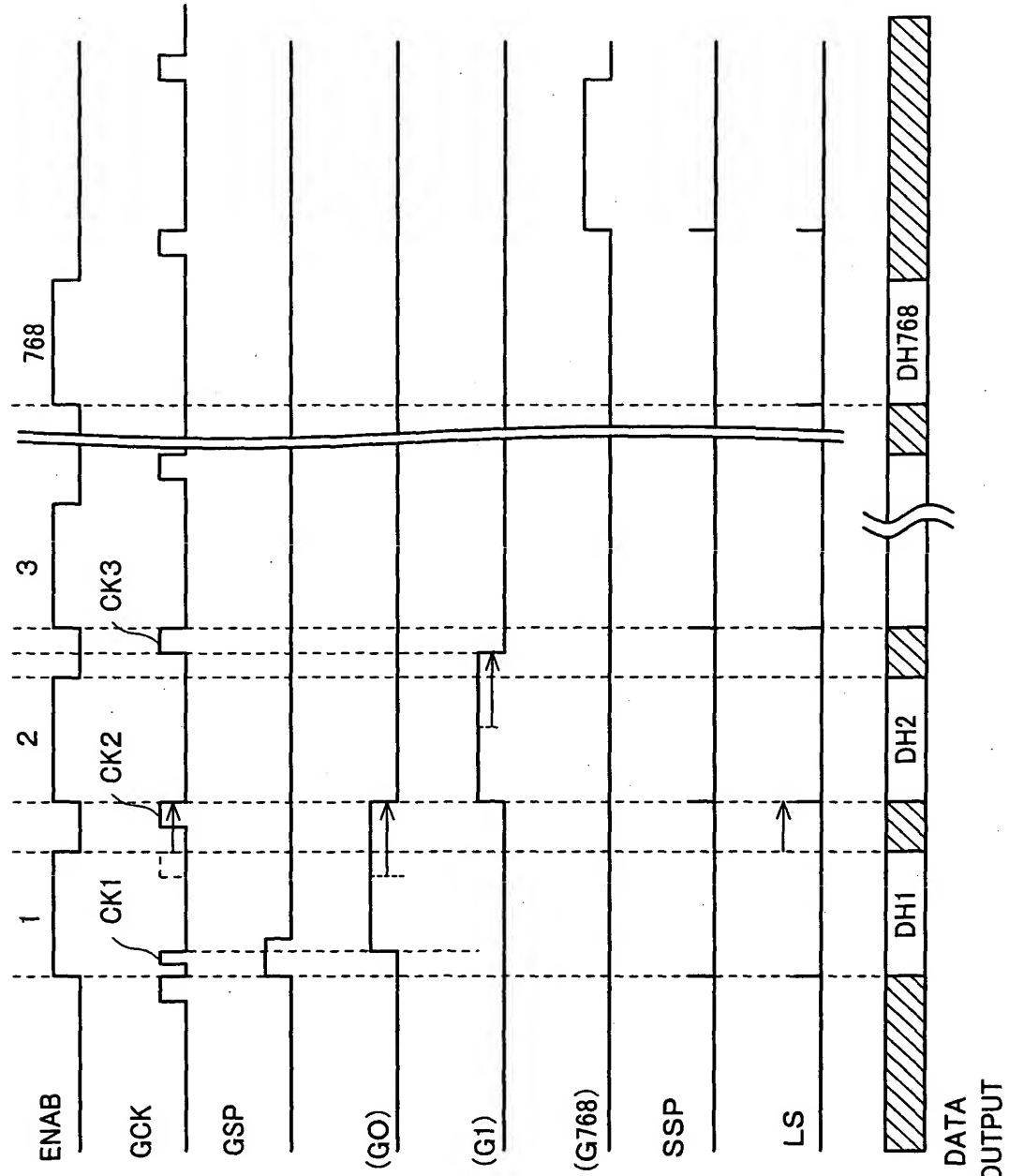


FIG. 11



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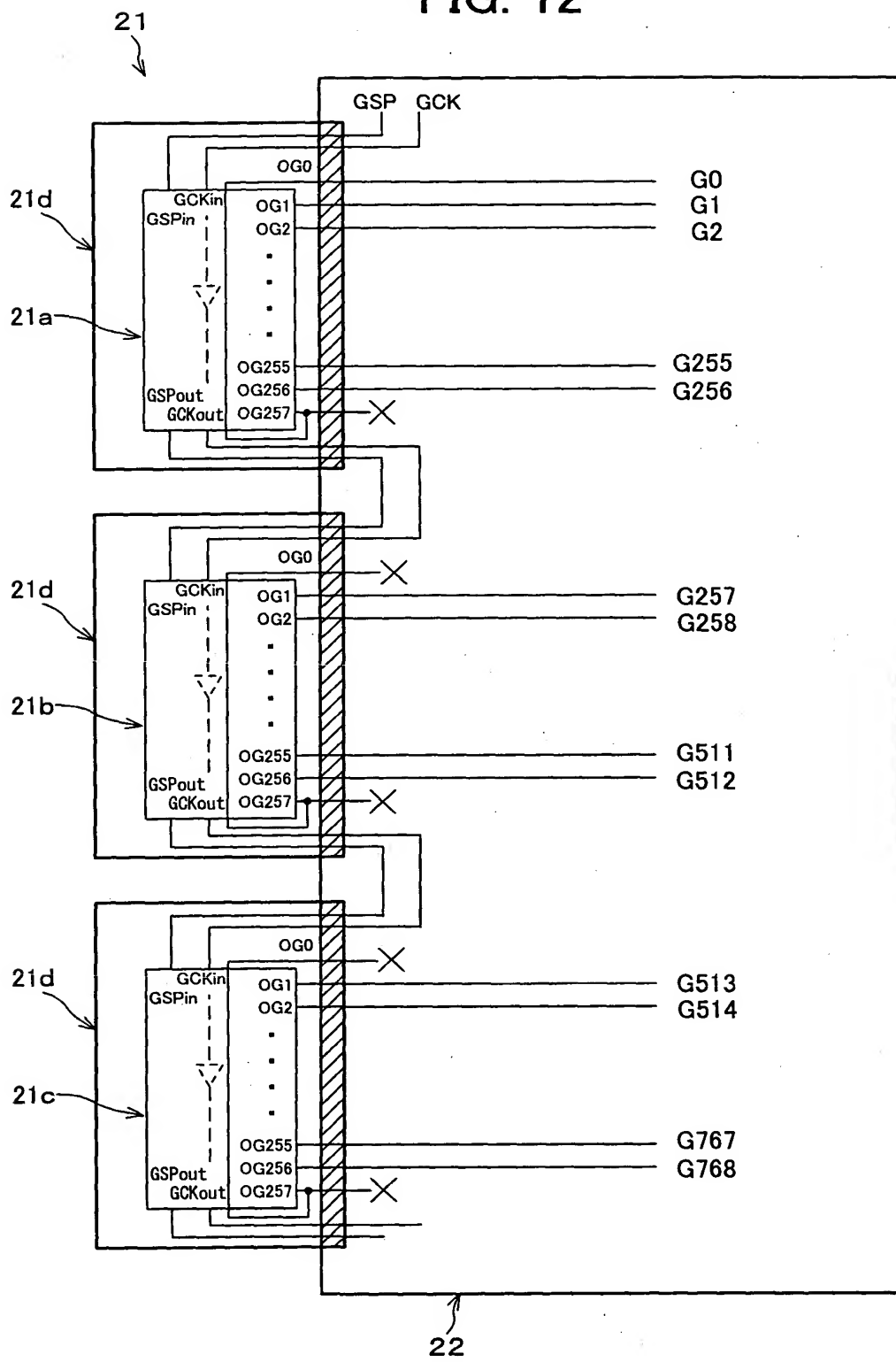
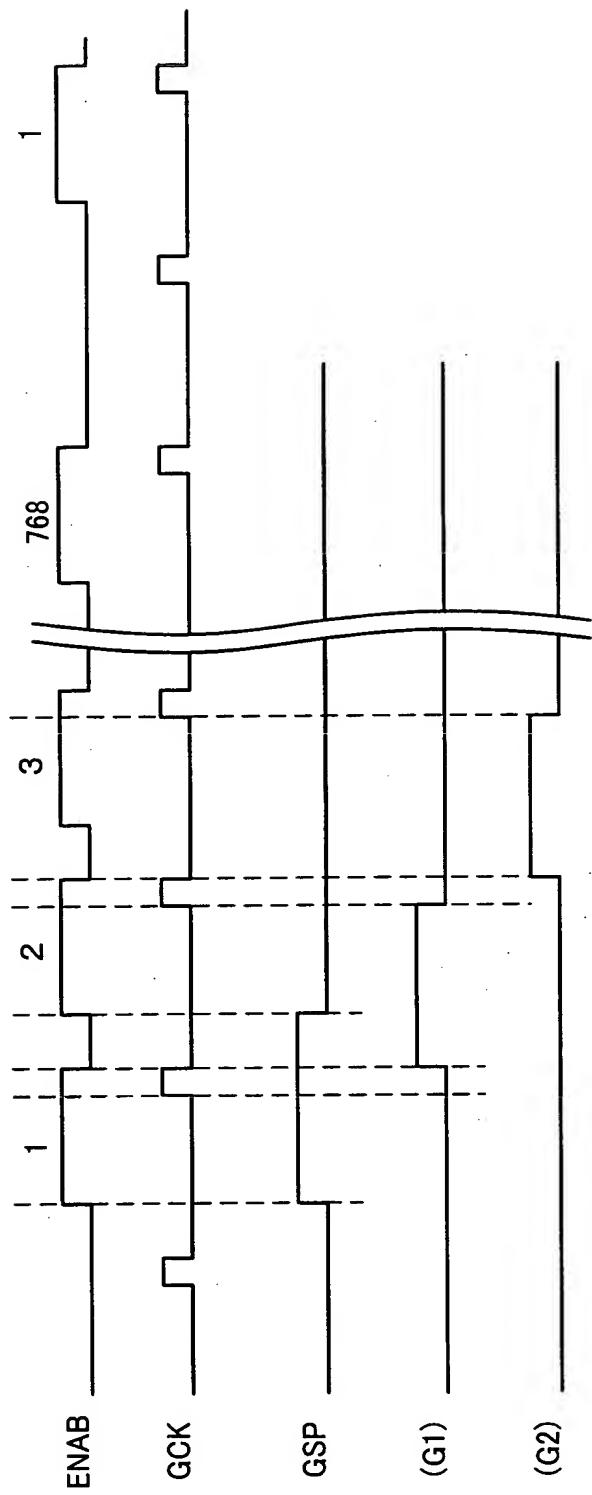


FIG. 13



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The diagram shows the timing of various signals relative to a common clock. The signals are:

- GCKin**: A clock signal with a period of 1 unit.
- GSPin**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG0**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG1**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG2**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG255**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG256**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- OG257**: A signal that transitions from low to high at the start of the first clock cycle and remains high.
- GSPout**: A signal that transitions from low to high at the start of the first clock cycle and remains high.

The diagram also shows a data bus signal (CK1 through CK259) that transitions from low to high at the start of the first clock cycle and remains high.

FIG. 15

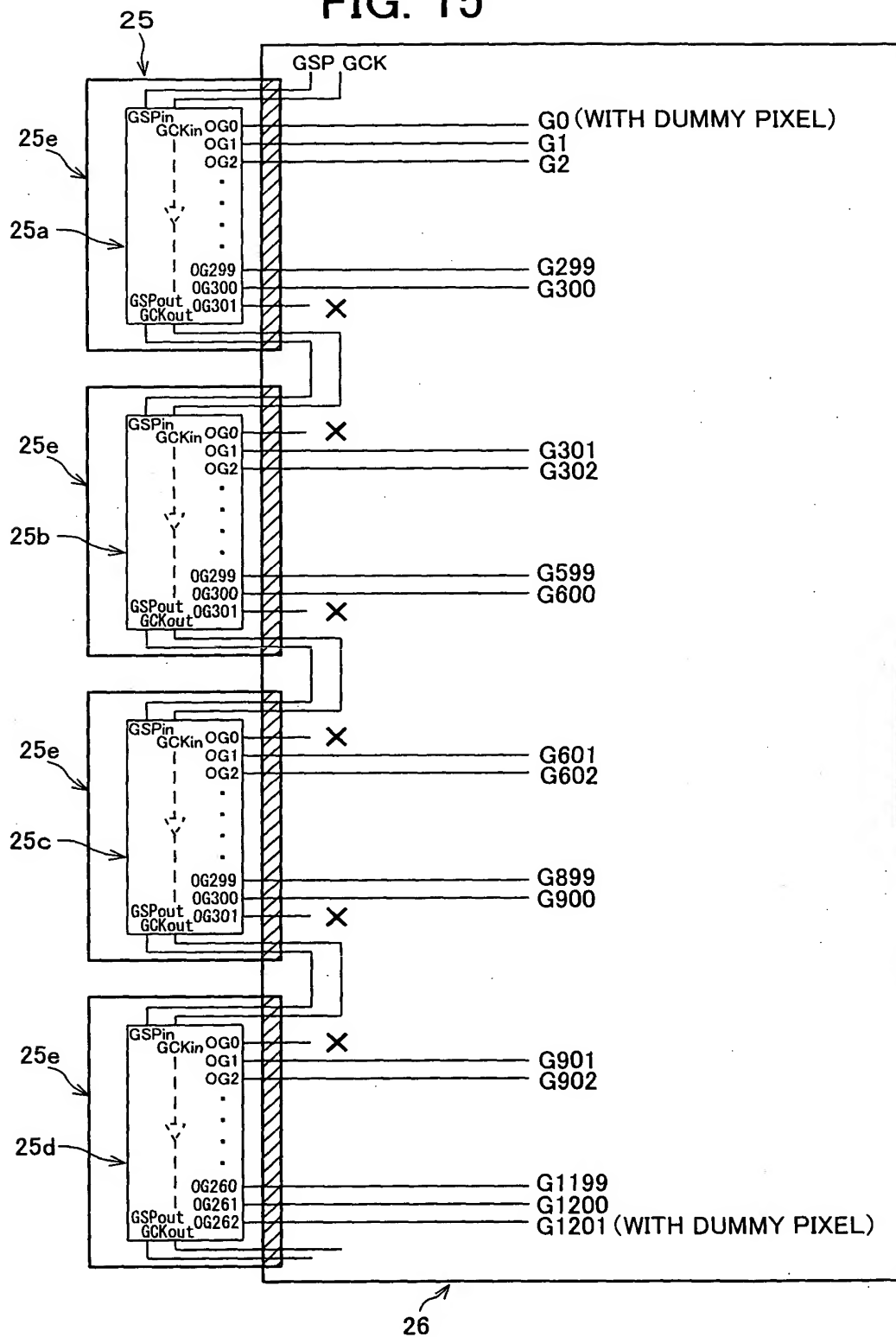
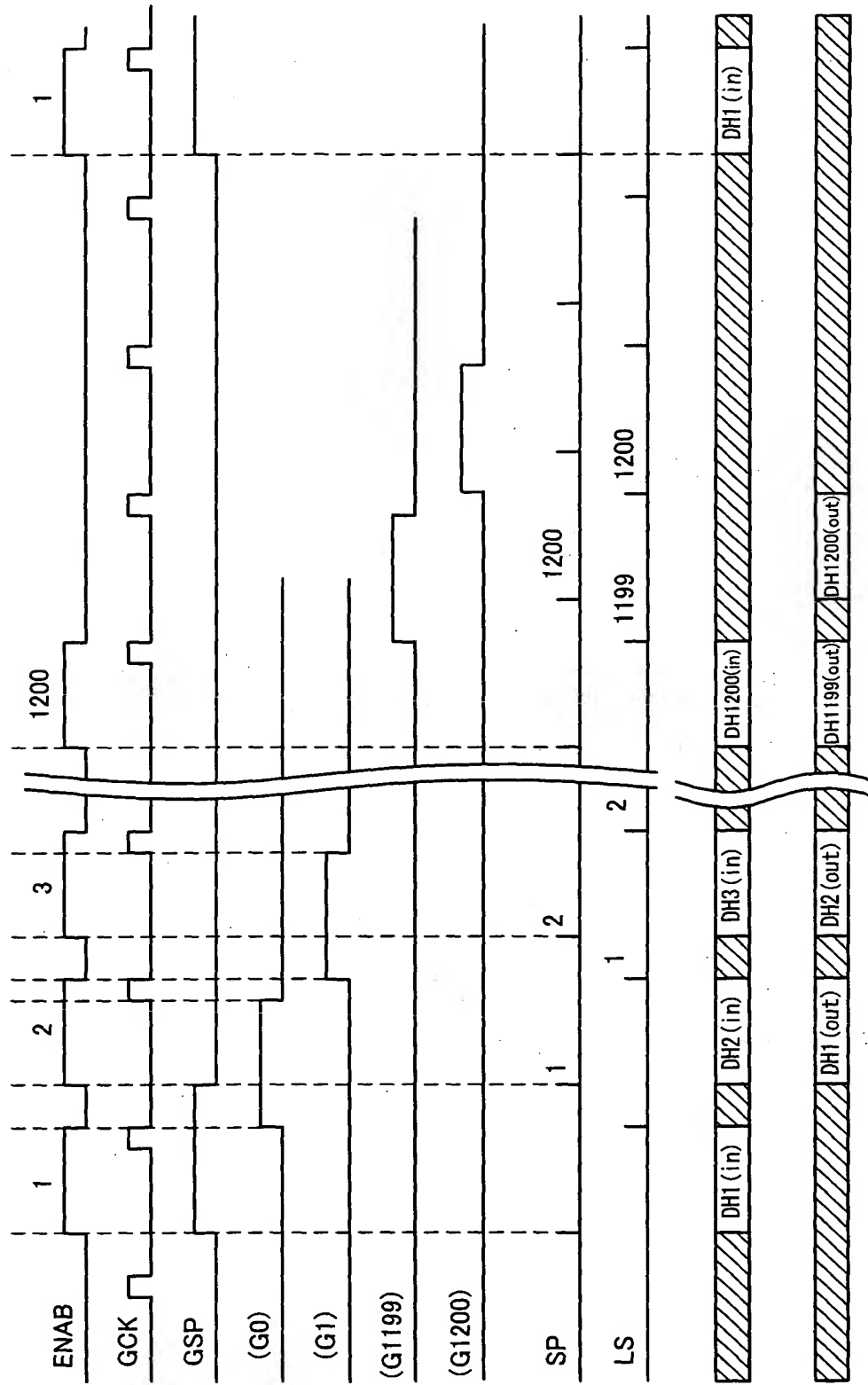


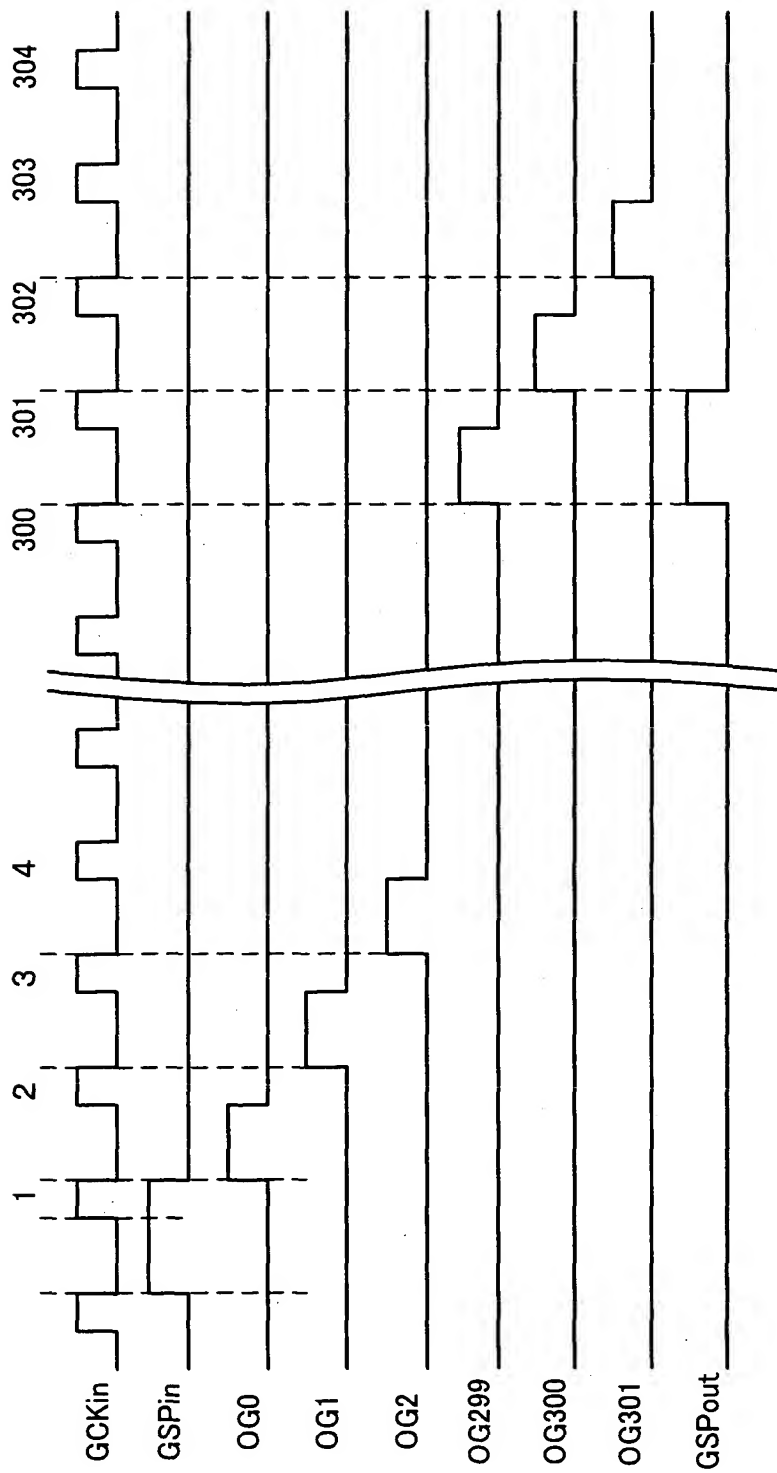
FIG. 16



The timing diagram illustrates the behavior of the GSP module across 304 time steps. The signals are as follows:

- GCKin:** A periodic square wave with a period of 2 steps, alternating between high and low.
- GSPin:** A square wave that is high from step 1 to 10 and low thereafter.
- OG0:** A square wave that is high from step 1 to 10 and low thereafter.
- OG1:** A square wave that is high from step 1 to 10 and low thereafter.
- OG2:** A square wave that is high from step 1 to 10 and low thereafter.
- OG299:** A square wave that is high from step 1 to 10 and low thereafter.
- OG300:** A square wave that is high from step 1 to 10 and low thereafter.
- OG301:** A square wave that is high from step 1 to 10 and low thereafter.
- GSPout:** A square wave that is high from step 1 to 10 and low thereafter.

The diagram includes a break in the timeline between step 4 and step 300, indicated by a wavy line. Vertical dashed lines mark the boundaries of the time steps.



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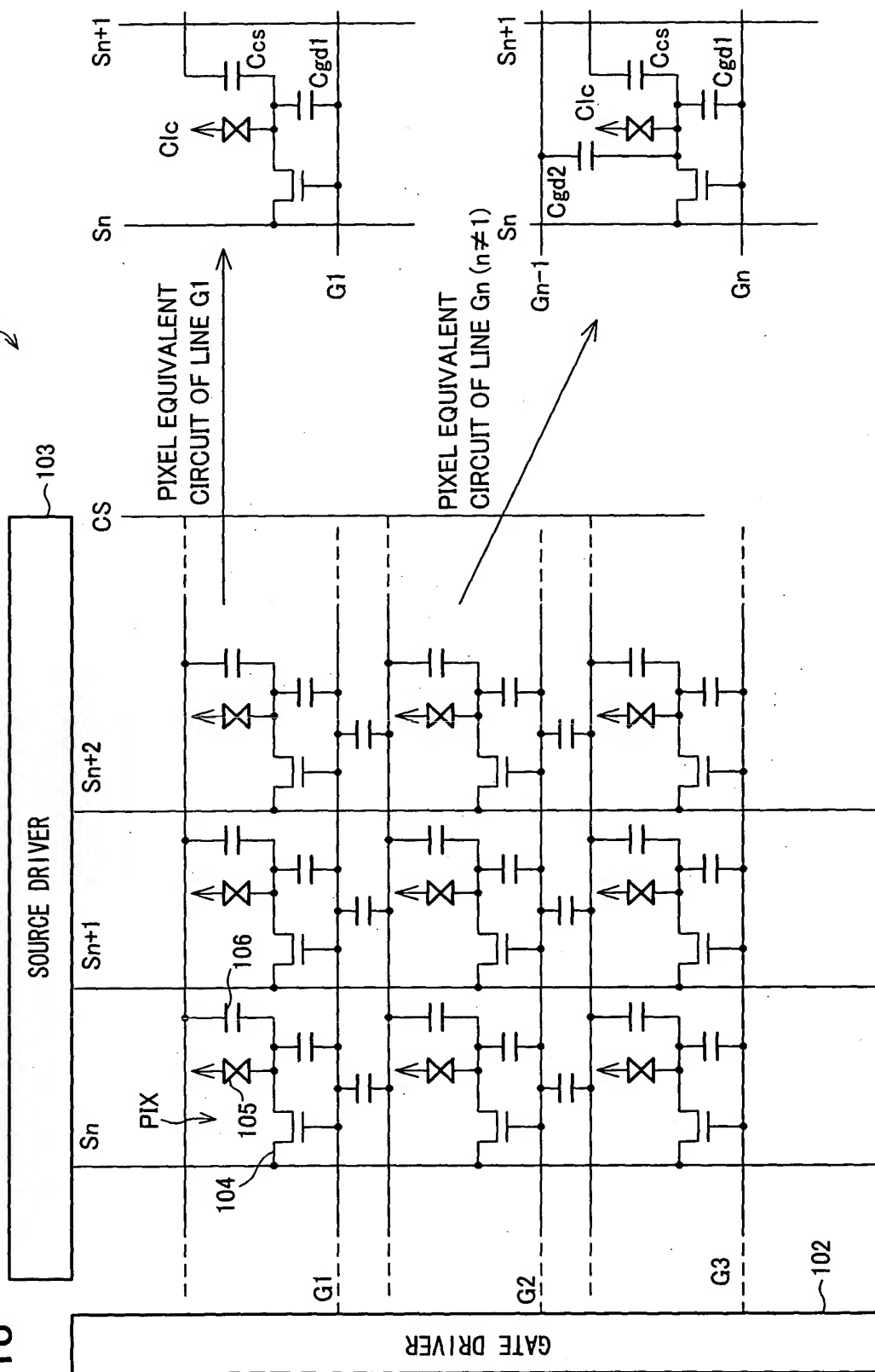


FIG. 19

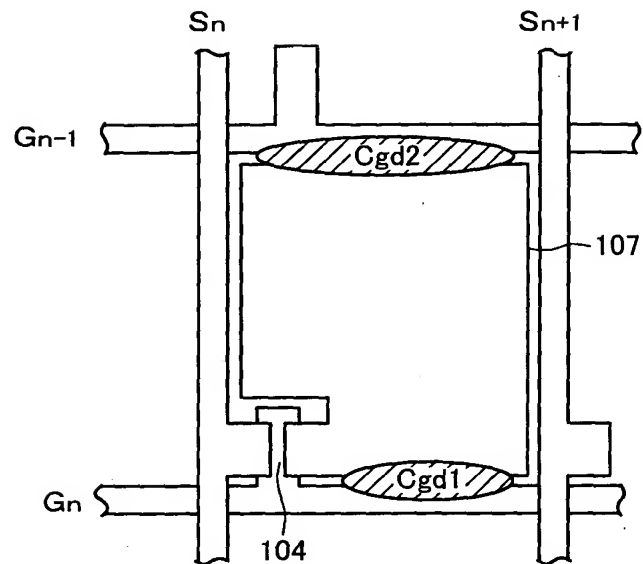


FIG. 20

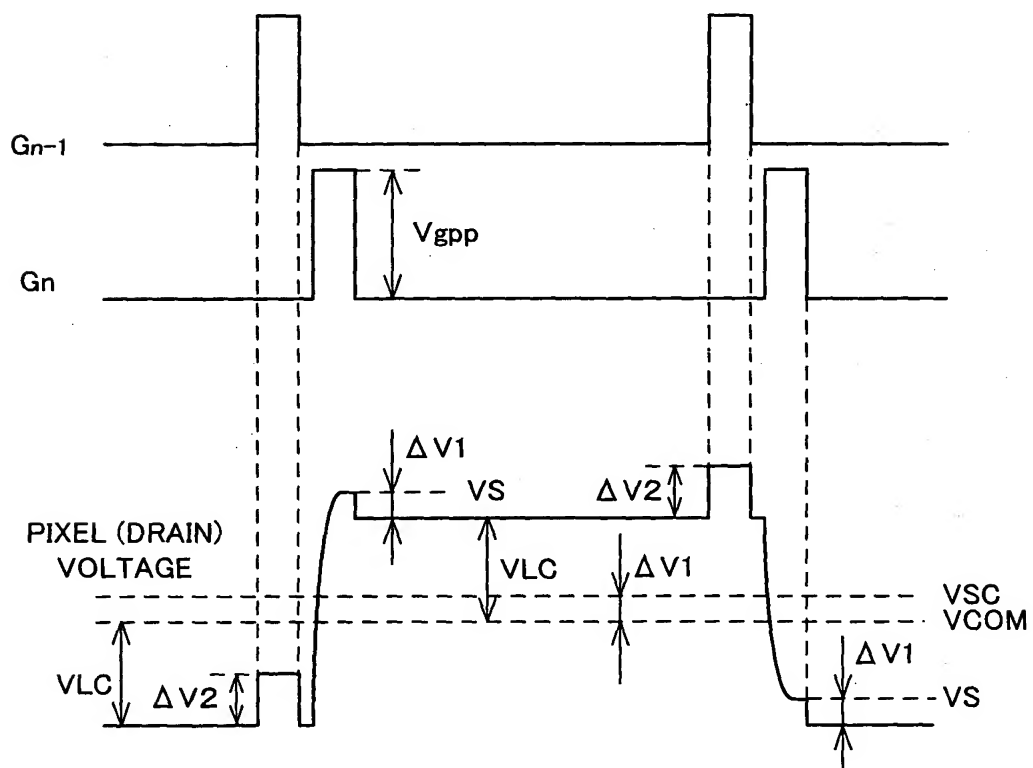
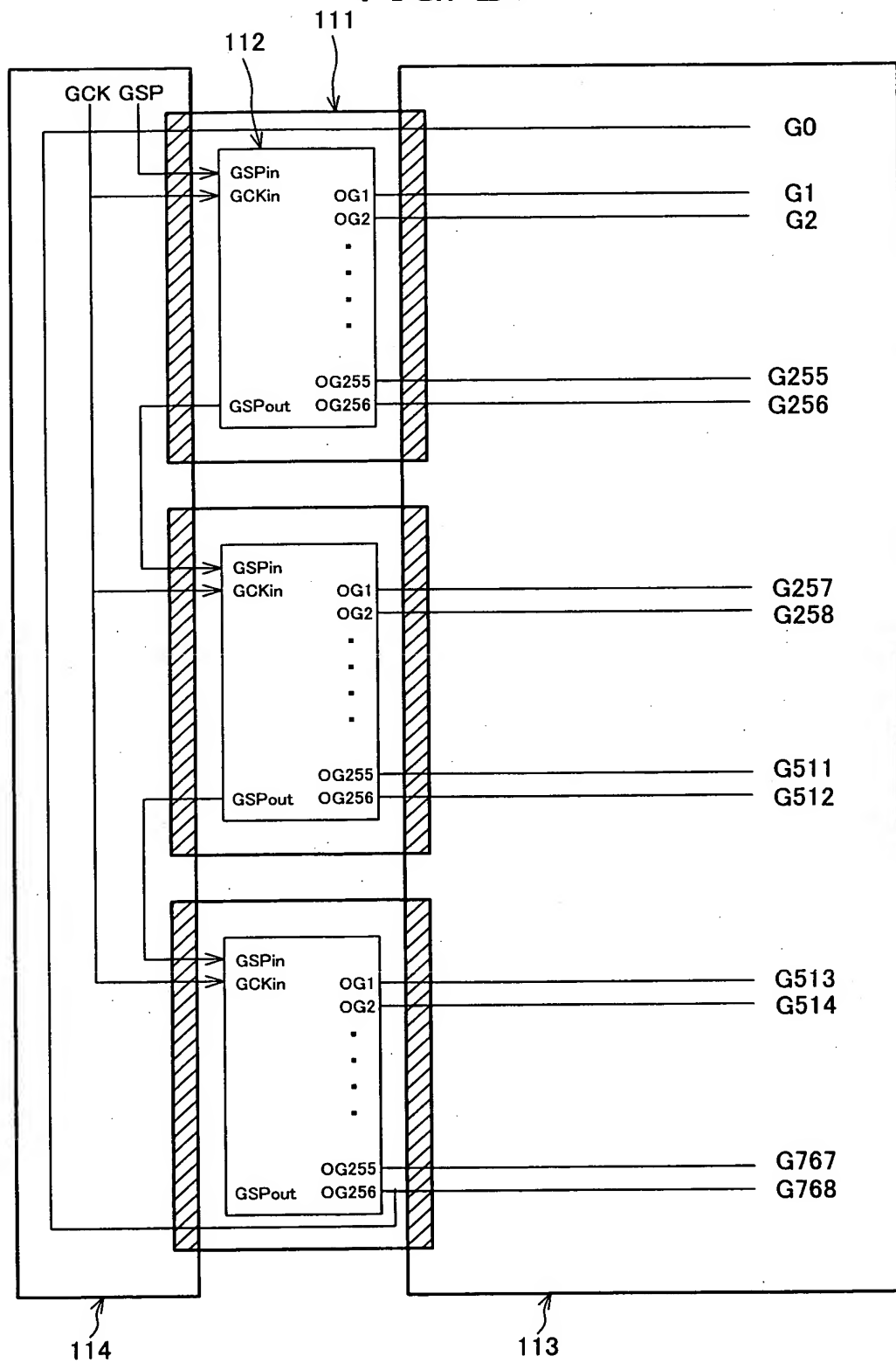


FIG. 21



The diagram shows the timing of various signals over 258 clock cycles. The signals are:

- GCKin**: Clock signal, periodic square wave.
- GSPin**: Serial data input, high for the first 10 cycles, then low.
- OG1**: Output 1, high for the first 10 cycles, then low.
- OG2**: Output 2, high for the first 10 cycles, then low.
- OG3**: Output 3, high for the first 10 cycles, then low.
- OG254**: Output 254, high for the first 10 cycles, then low.
- OG255**: Output 255, high for the first 10 cycles, then low.
- OG256**: Output 256, high for the first 10 cycles, then low.
- GSPout**: Serial data output, high for the first 10 cycles, then low.

A thick line indicates a data bus or control signal, which is high for the first 10 cycles and then low.

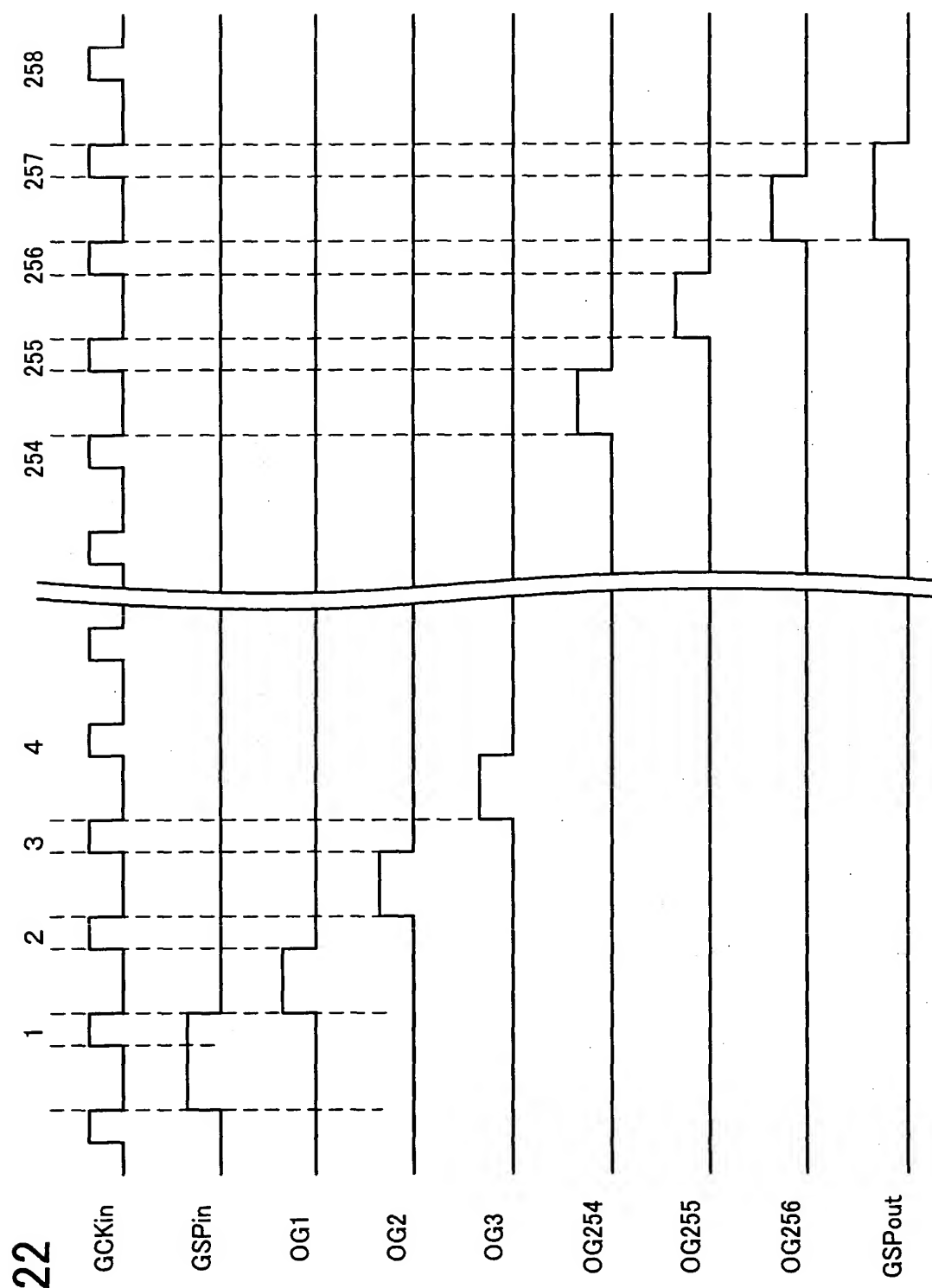


FIG. 23

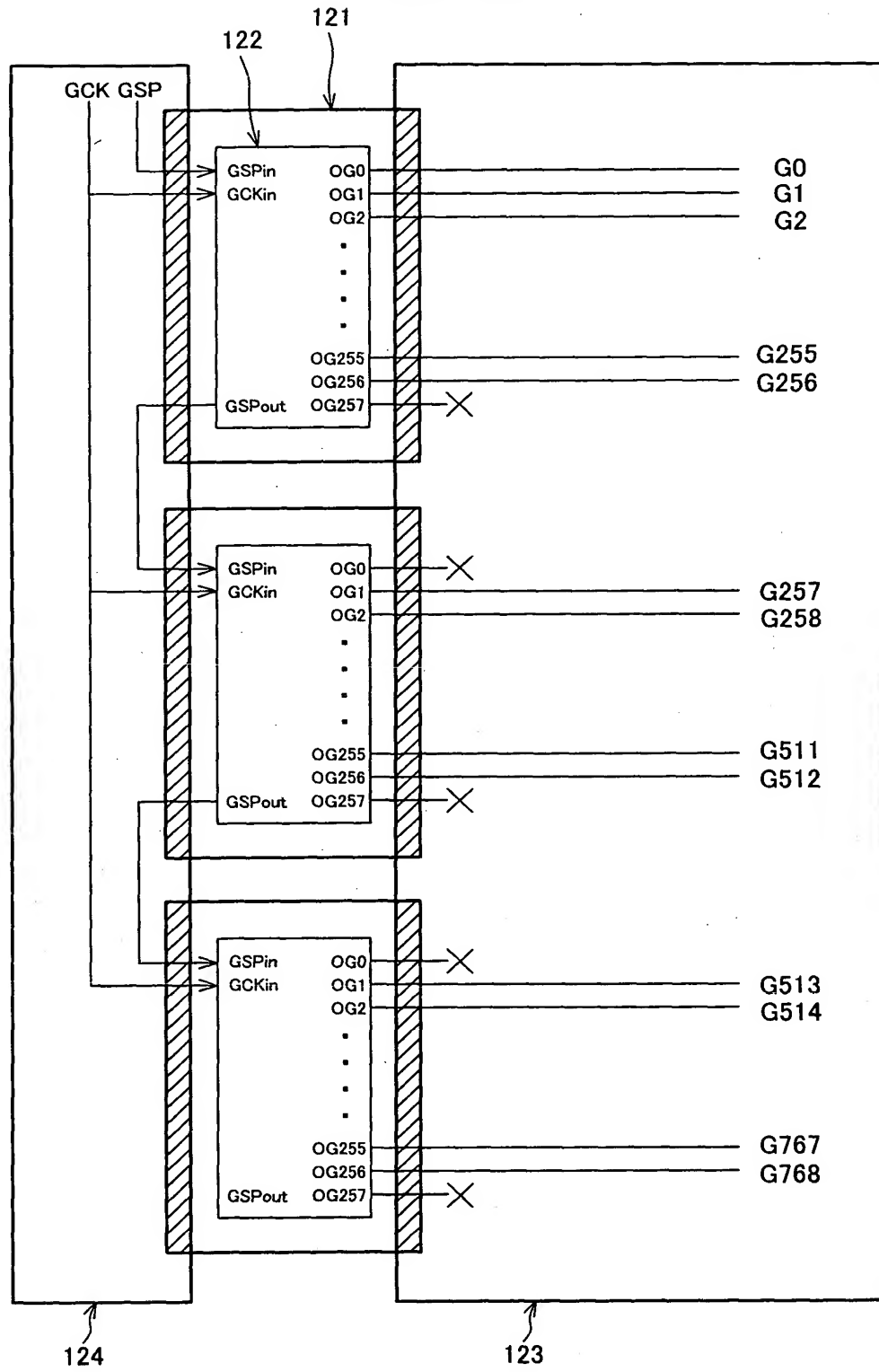


FIG. 24

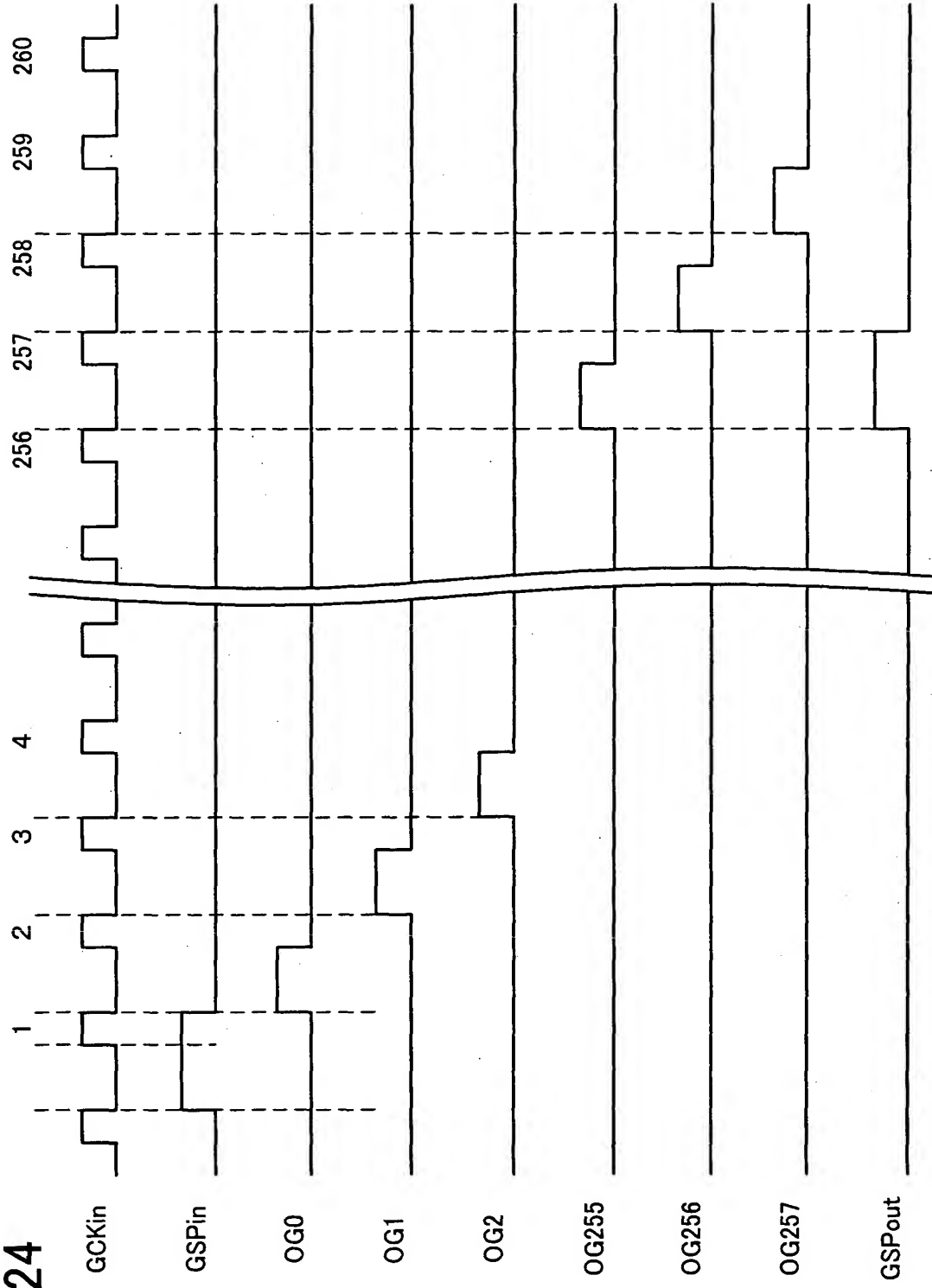


FIG. 25

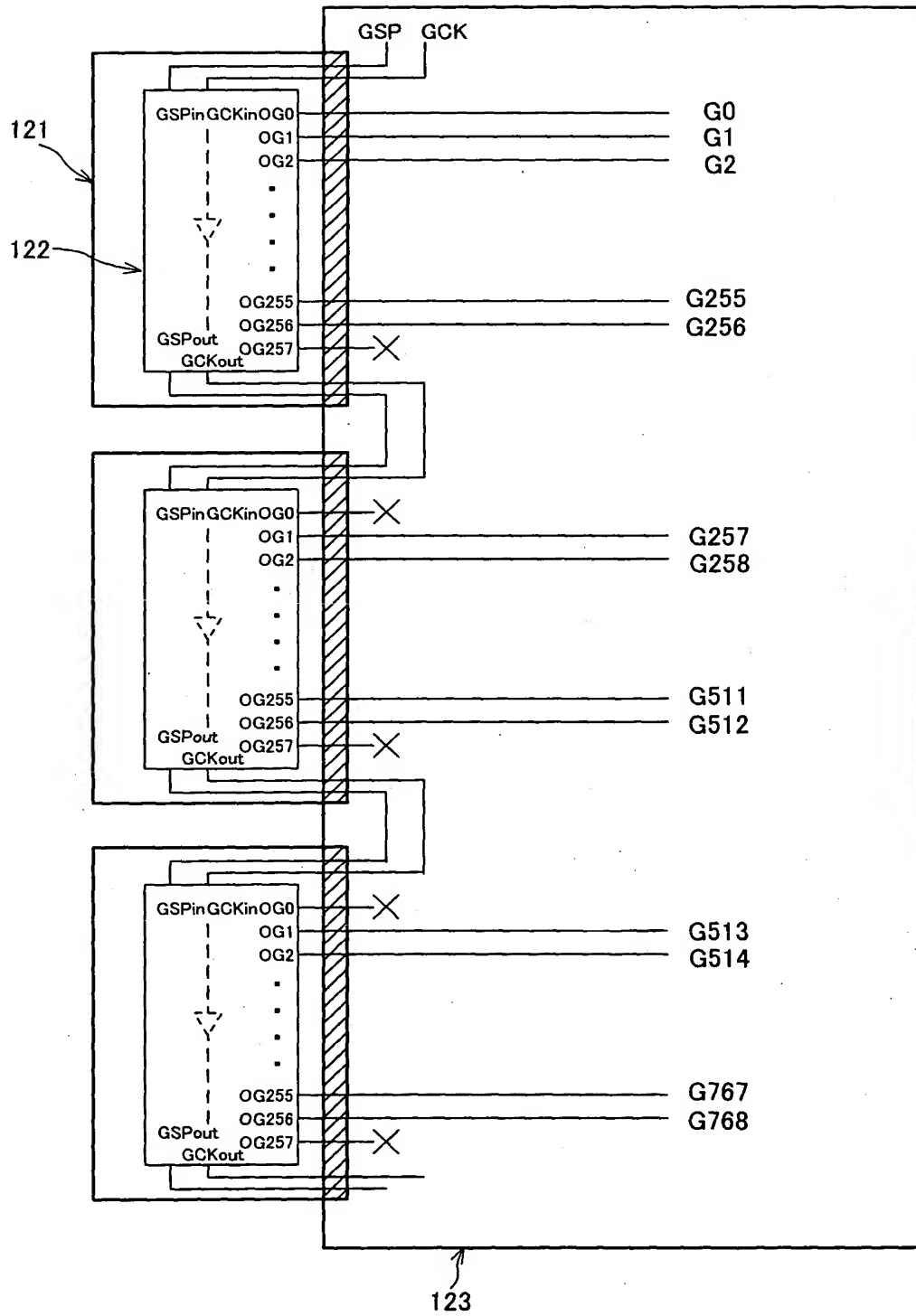


FIG. 26 (a)

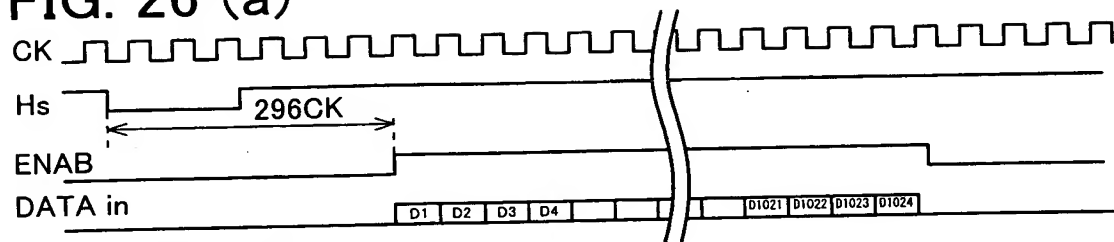


FIG. 26 (b)

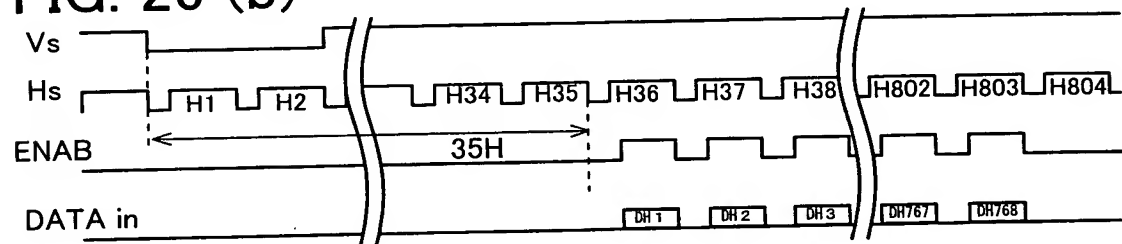


FIG. 26 (c)

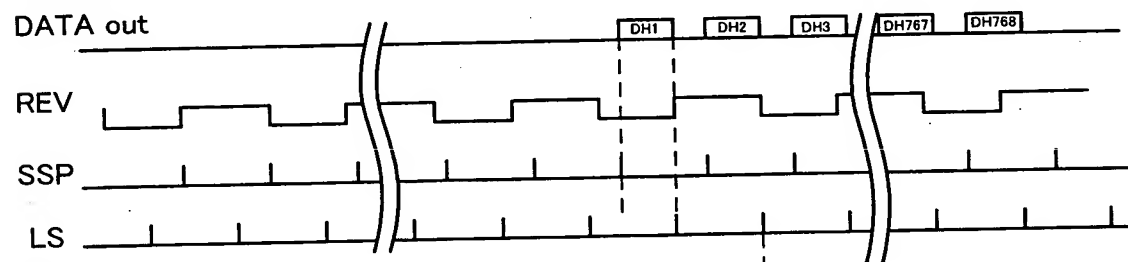


FIG. 26 (d)



FIG. 26 (e)

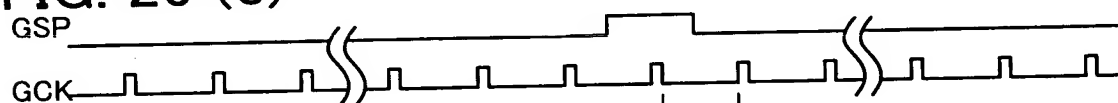


FIG. 26 (f)

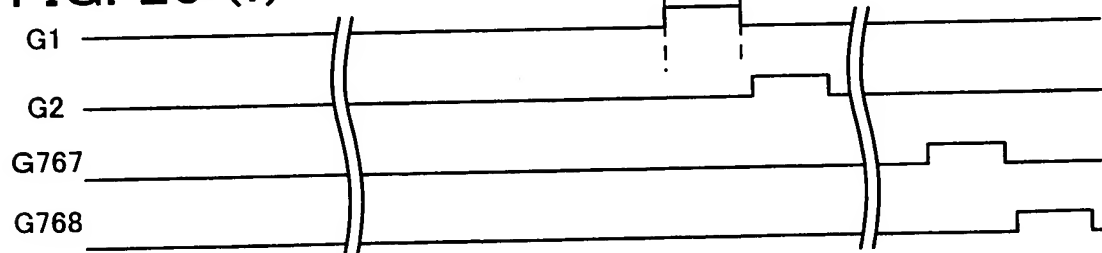


FIG. 27 (a)

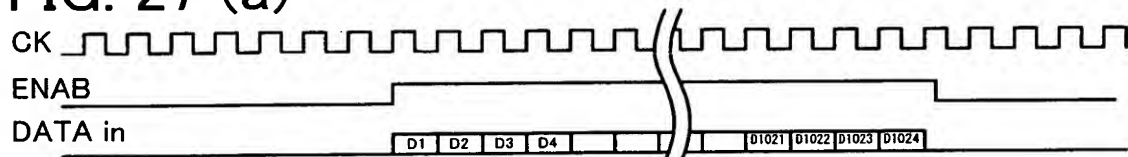


FIG. 27 (b)

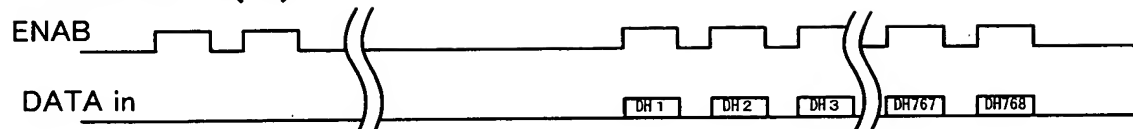


FIG. 27 (c)

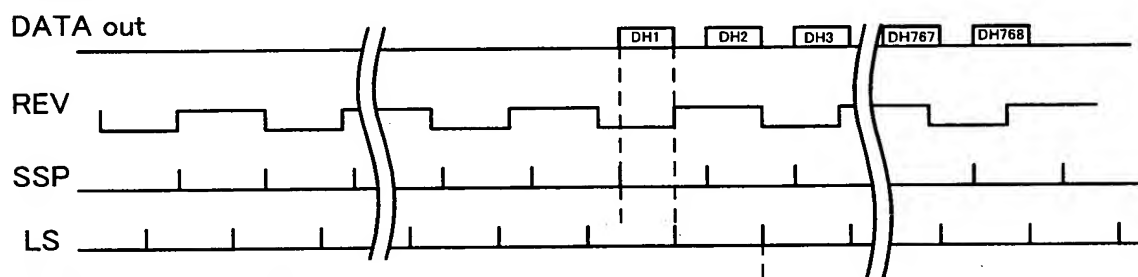


FIG. 27 (d)

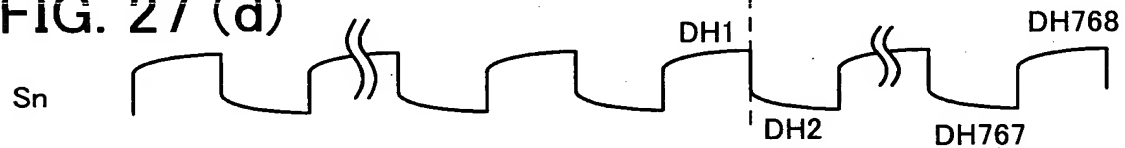


FIG. 27 (e)

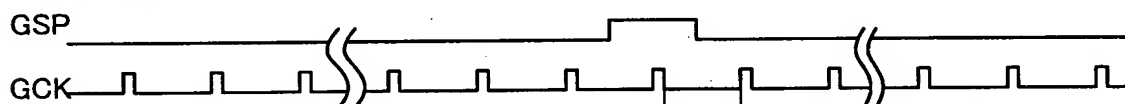


FIG. 27 (f)

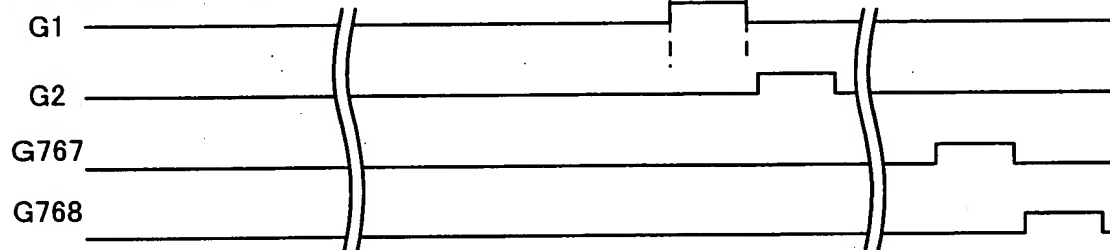


FIG. 28

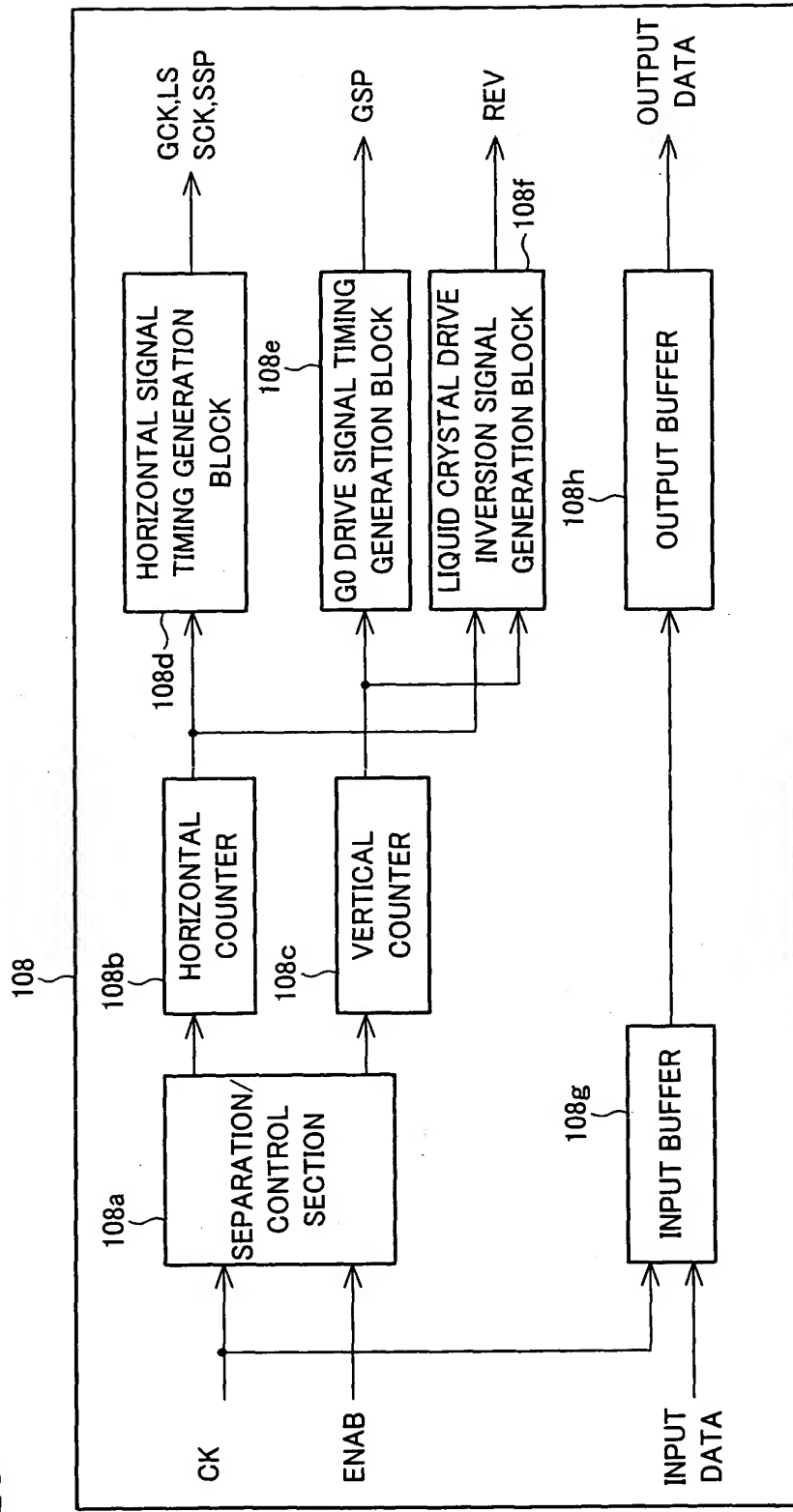


FIG. 29

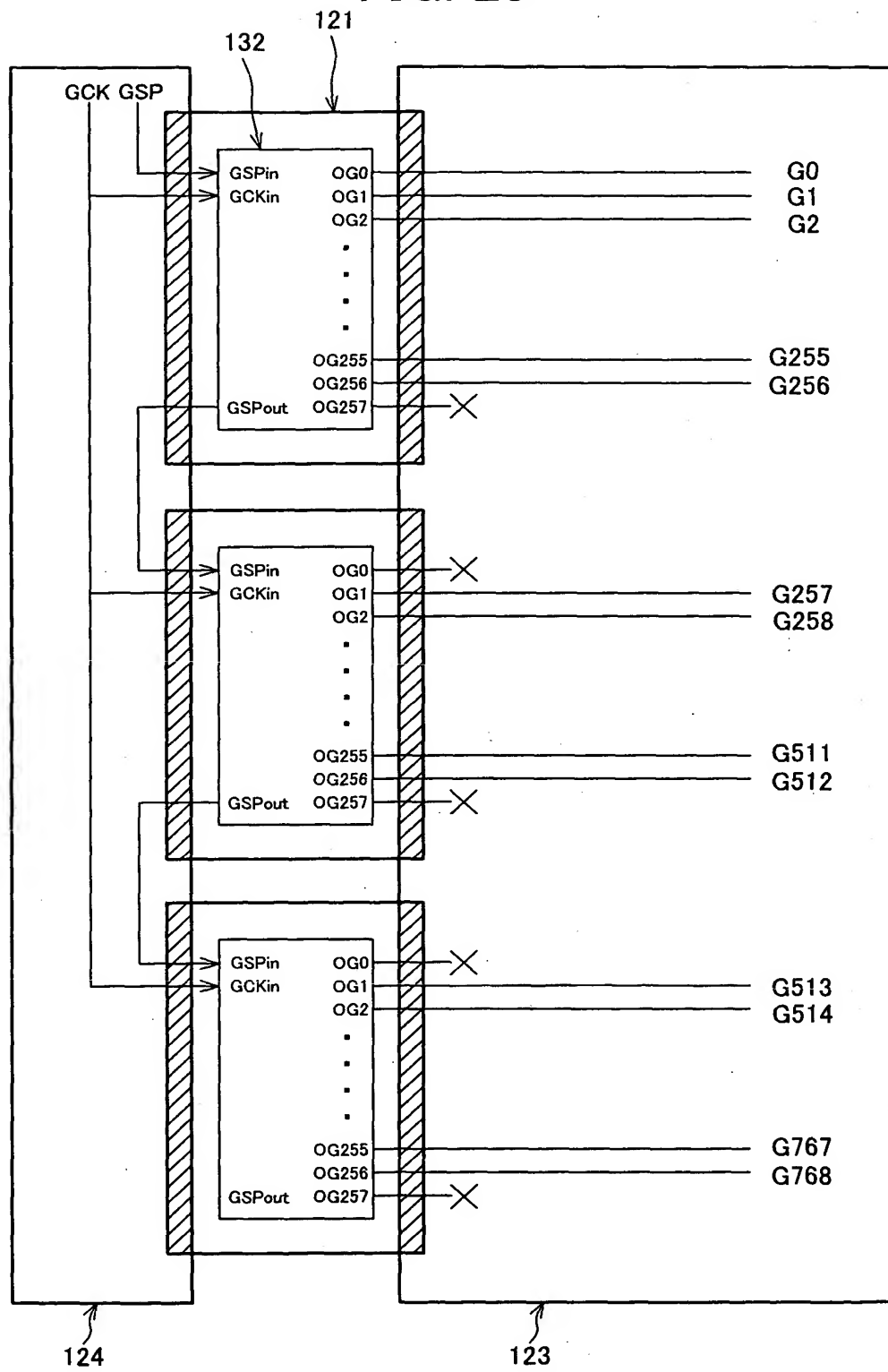


FIG. 30

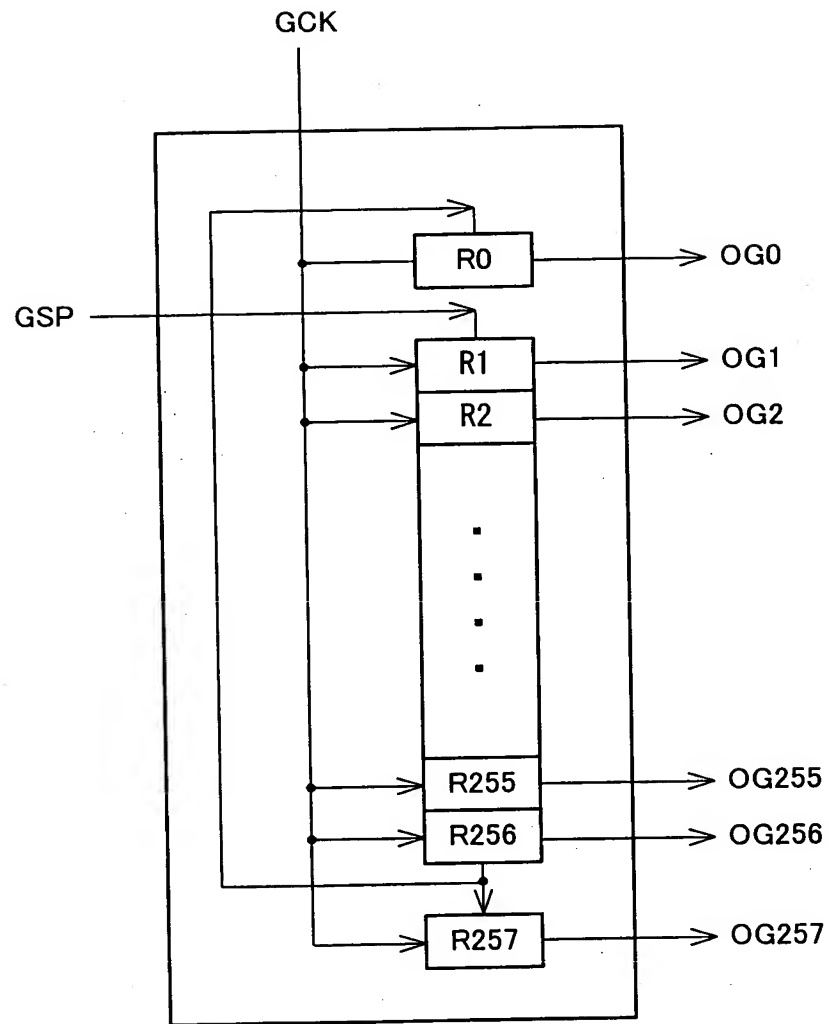


FIG. 31

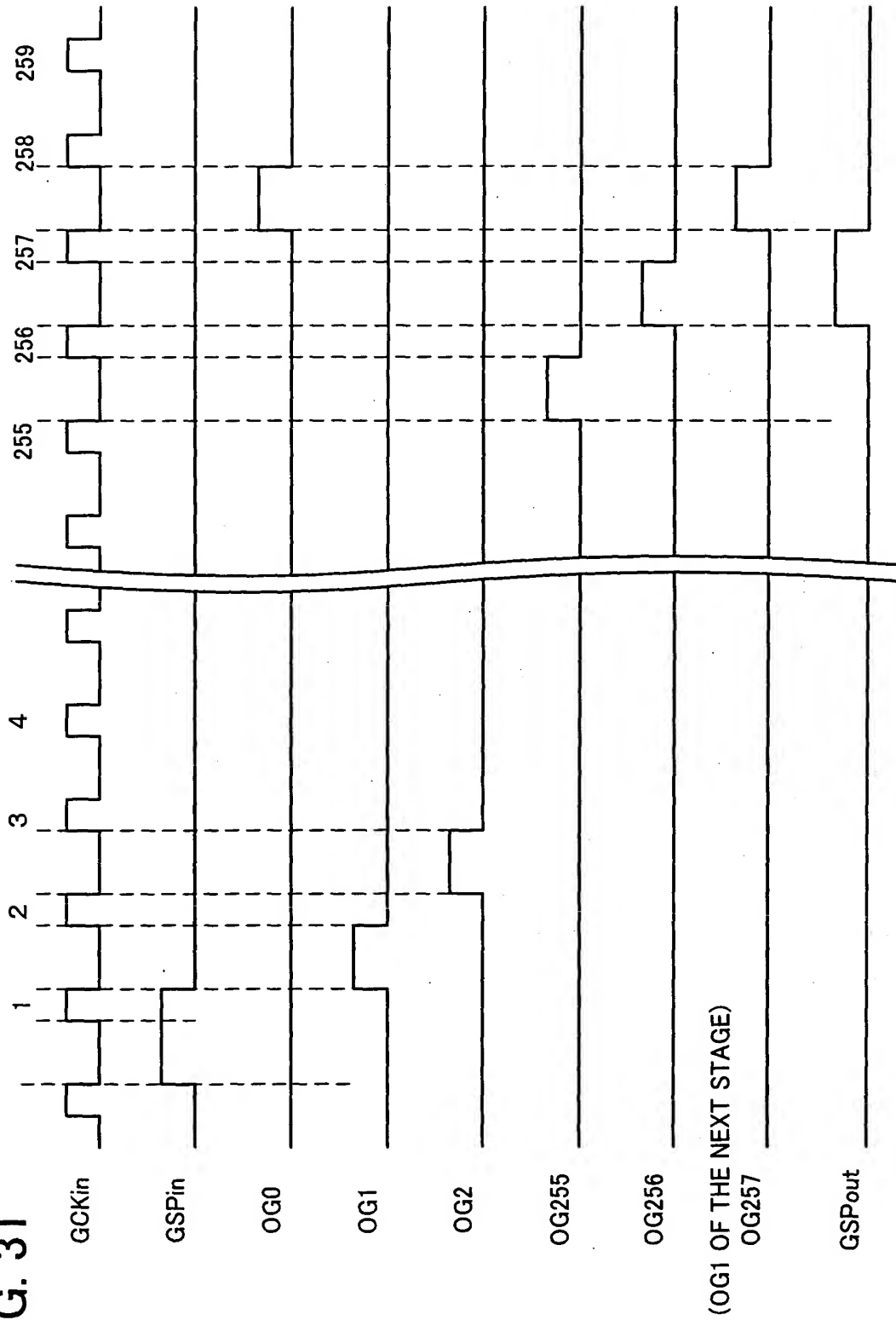


FIG. 1

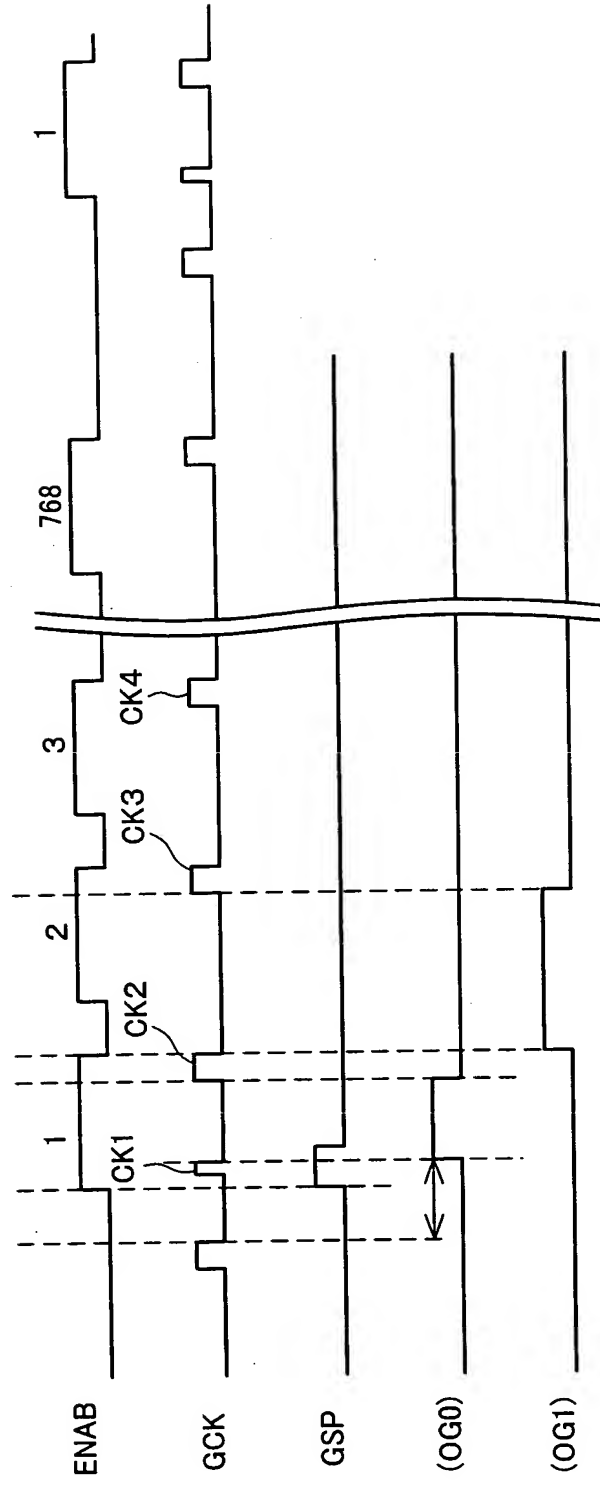


FIG. 2

